CLAIMS

1. In combination, plural integrated circuit chips, clock circuitry for supplying synchronized clock waves to loads on the plural integrated circuit chips, the clock circuitry being on the chips and adapted to be responsive to a source of clock waves, the clock circuitry being arranged for coupling the synchronized clock waves to regions of the plural chips, first and second routes for the clock waves between pairs of the chips, the first and second routes and the chips being arranged so there is a first clock wave route in a first direction from a first chip of a particular pair to a second chip of that particular pair, and a second clock wave route in a second direction from the second chip of the particular pair to the first chip of the particular pair, the first and second routes having substantially the same geometry and being in close proximity to each other so they have substantially the same effects on clock waves propagating therein in opposite directions, and circuitry for maintaining a substantially constant phase relation between the clock waves transmitted to and from the first chip via the first and second routes.

2. The combination of claim 1 wherein the circuitry is on the first chip.

3. The combination of claim 1 wherein the circuitry is on a third chip and the circuitry is arranged for deriving a control signal for maintaining the substantially constant phase relation, and further including signal transmission circuit elements for coupling the signal from the third chip to the first and second chips.

4. The combination of claim 3 wherein the signal transmission elements include a common mode path for the control signal between the third chip and the first and second chips.

5. The combination of claim 4 wherein the circuitry includes a phase detector connected to be responsive to a clock wave on the third chip and a clock wave adapted to propagate from the third chip back to the third chip via routes between a plurality of the chips.

6. The combination of claim 5 wherein the circuitry for maintaining a substantially constant phase relation includes variable delay circuits for the clock waves, the variable delay circuits being arranged to be responsive to the signal on the common mode path.

7. The combination of claim 3 wherein the circuitry includes a phase detector connected to be responsive to a clock wave on the third chip and a clock wave adapted to propagate from the third chip back to the third chip via routes between a plurality of the chips.

8. The combination of claim 7 wherein the circuitry for maintaining a substantially constant phase relation includes variable delay circuits for the clock waves, the variable delay circuits being arranged to be responsive to the signal on the common mode path.

9. The combination of claim 1 wherein the circuitry includes a phase detector connected to be responsive to a clock wave on the first chip and a clock wave adapted to propagate from the first chip back to the first chip via routes between a plurality of the chips.

10. The combination of claim 9 wherein the circuitry for maintaining a substantially constant phase relation includes variable delay circuits for the clock waves, the variable delay circuits being arranged to be responsive to a signal derived by the phase detector indicative of the differences in phase of the clock waves connected to drive the phase detector.

11. The combination of claim 1 further including circuitry for determining the phase difference between the clock wave supplied to one of the plural integrated circuit chips and clock waves adapted to propagate from the one chip to additional chips connected to be sequentially responsive to the clock wave derived from the one chip.

12. The combination of claim 11 wherein the circuitry for determining is arranged to derive an error signal, a path for the error signal to at least some of the chips, the chips having (a) connections to the path for the error signal and (b) a variable delay element arranged to have a delay time adapted to be controlled by the error signal.

13. The circuitry of claim 11 wherein the circuitry for determining is arranged to derive an output signal having a value indicative of clock quality, said clock quality signal having no control effect on the plural integrated circuit chips.

14. The combination of claim 1 wherein the plural chips are connected to each other in sequence and arranged for causing the clock waves to propagate via said routes in sequence from chip i to chip (i+1) via route i, where i is sequentially 1... (N-1) and N is the number of chips.

15. The combination of claim 1 wherein the chips are connected to each other via the routes so that the chips are connected in a star configuration.

16. The combination of claim 1 wherein the chips and routes are carried by a circuit board.

17. The combination of claim 1 wherein the chips are stacked on each other and the routes comprise vias in and between the chips.